Direct Conversion Radio for Digital Mobile Phones—Design Issues, Status, and Trends

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Invited Paper

***Abstract*—Applications of direct frequency-conversion techniques have been rapidly getting attention of radio designers worldwide. This paper focuses on bringing out key implementation challenges of direct conversion receivers and transmitters targeted for different second- and third-generation mobile phone standards like global system for mobile communication, code division multiple access (cdmaOne and CDMA 2000), and wide-band code division multiple access. Techniques and tradeoffs to arrive at optimal implementation are highlighted. Some of the commercially available application-specific integrated circuits that are based on direct conversion architecture and their salient features are summarized.**

***Index Terms*—Code division multiple access (CDMA), direct conversion radio, global system for mobile communication (GSM), mobile communication, wide-band code division multiple access (WCDMA).**

I. Introduction

OVER THE PAST several years, the mobile-phone market has experienced a significant growth. As the industry transitions from second generation (2G) to third generation (3G), the phones are becoming more application and feature rich. These new small-size phones not only support the basic voice feature in multiple frequency bands, but also support high-speed data, multimedia applications, global positioning system (GPS) location technology, and Bluetooth (BT) wireless connectivity. The RF section of these new phones has experienced significant size reductions (Fig. 1) due to evolution of radio architectures, enabling semiconductor integrated circuit (IC) technologies, and innovative system and circuit design techniques

Increased pressure for small form factor, low cost, reduced bill of materials, and low power consumption in radio applications of mobile phones have triggered the industry to resurrect the direct conversion transceiver radio architecture. Long abandoned in favor of mature super heterodyne architecture, direct frequency conversion has emerged over the last four years as the de-facto standard for global system for mobile communication (GSM) handset design. Active research and application-specific integrated circuit (ASIC) implementations are being currently pursued to develop direct-conversion radio architecture also for wide-band code division multiple access (WCDMA) and code division multiple access (CDMA) handsets.

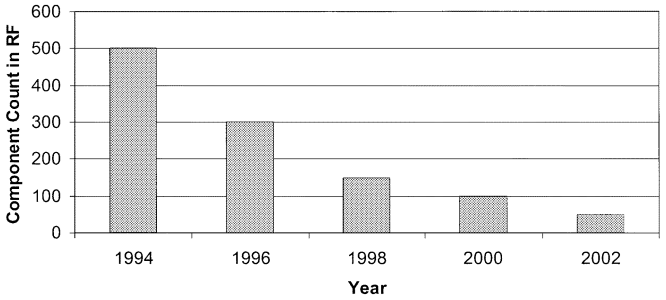

Fig. 1. RF component count reduction in GSM mobile handsets over the years.

Various digital cellular systems [GSM, CDMA, WCDMA, time division multiple access (TDMA)] that evolved over time in different parts of the world differ from each other in frequency bands, modulation schemes, channel bandwidth, duplex spacing, etc. (Table I) and have distinct RF system requirements (e.g., sensitivity, input third-order intercept point (IIP3), input second-order intercept point (IIP2), phase noise, output power, adjacent channel power ratio (ACPR), local oscillator (LO) leakage).

This paper describes direct-conversion receiver (DCR) and transmitter design issues, as related to system requirements of GSM, WCDMA, and CDMA protocols. The current U.S. TDMA-based mobile-phone protocol is not covered in this paper, as that system is targeted for migration to GSM/WCDMA by 2003. A brief overview of the general merits of DCR and direct-conversion transmitter (DCT) are presented in Section II. Implementation challenges and tradeoffs of direct-conversion transceivers for these mobile phones, and popular approaches for circumventing DCR/DCT related issues are presented in Section III and IV. Specific examples of current direct conversion transceiver ICs developed by different companies are summarized in Section V.

II. DCR and DCT: A New Paradigm

A. DCR

In a DCR, the incoming RF signal is amplified by a low-noise amplifier (LNA) and then directly demodulated to baseband in-phase (I) and quadrature (Q) signals. Channel selection and

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TABLE I
MAIN DIGITAL CELLULAR SYSTEMS

	GSM			CDMA 2K		WCDMA
	EGSM	DCS	PCS	Cell	PCS	Europe
Parameter						
Forward Link (MS Rx)	925-960	1805-1910	1930-1990	869-894	1930-1990	2110-2170
Reverse Link (MS Tx)	880-915	1710-1785	1850-1910	824-849	1850-1910	1920-1980
Channel spacing	200 KHz			1.25 MHz		5 MHz
Multiple Access	Time Division Multiple Access			Code Division Multiple Access		
Duplexing	Frequency Division Duplexing					
Duplex Spacing (MHz)	45	95	80	45	80	80
Diversity	Frequency Hopping			Time Diversity / Space diversity		
Modulation FW link	GMSK 0.3			Quadrature PSK		Quadrature PSK
Modulation R Link				Hybrid PSK		Hybrid PSK
Signal Crest factor (FW Link)	Constant envelope			12-16 dB		12-16 dB
Dynamic Range	78 dB			80 dB		80 dB
Source coding (voice)	RPELTP			EVRC		AMR
Channel coding	Convolutional			Convolutional/ Turbo		Convolutional / Turbo
Data rate	12.2Kbps			307KBPS		2MBPS
Frequency re use factor	1-18			1		1

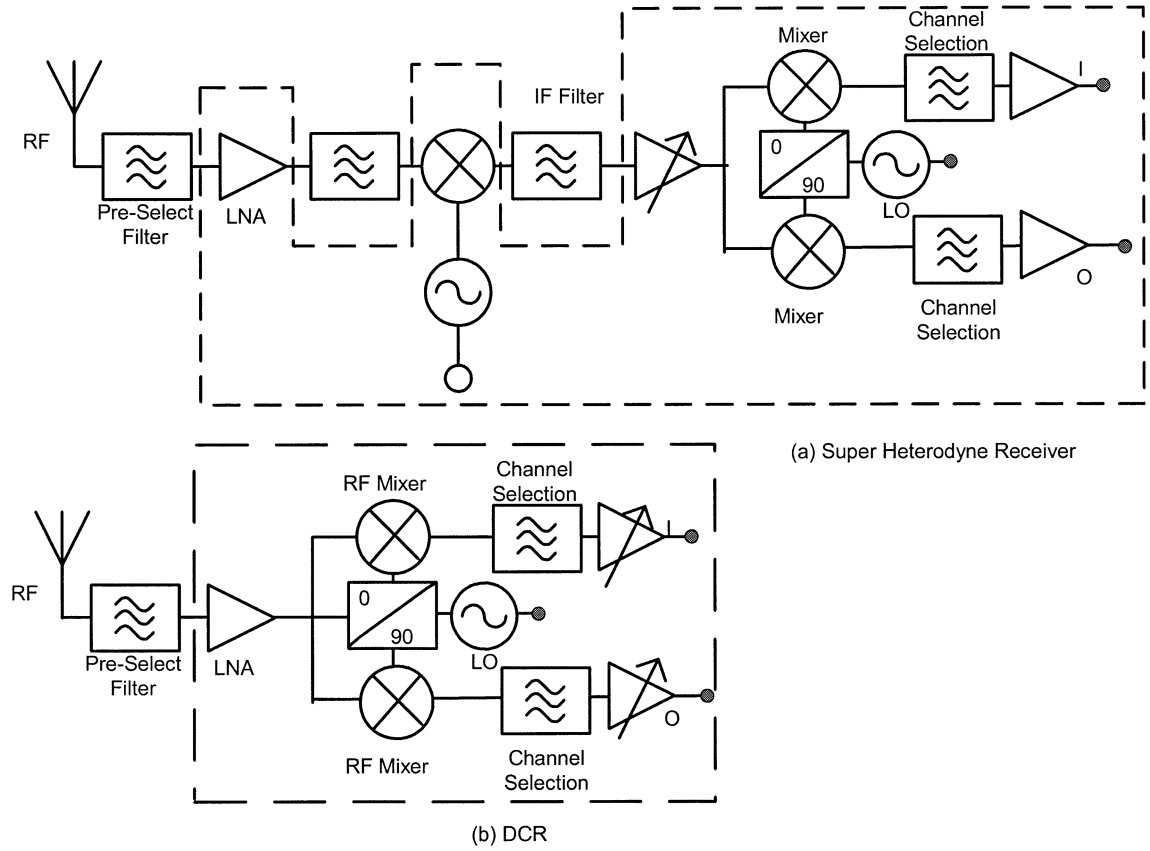

Fig. 2. Super-heterodyne and DCR architectures.

gain control are achieved by on-chip low-pass filters and variable gain amplifier (VGA) at baseband. Channel selectivity in super-heterodyne receivers is achieved by down-converting the RF signal to fixed IF and passing through an IF surface acoustic wave (SAW) (or crystal) filters [see Fig. 2(a)]. Receiver operating in multiple bands/standards may have different frequency

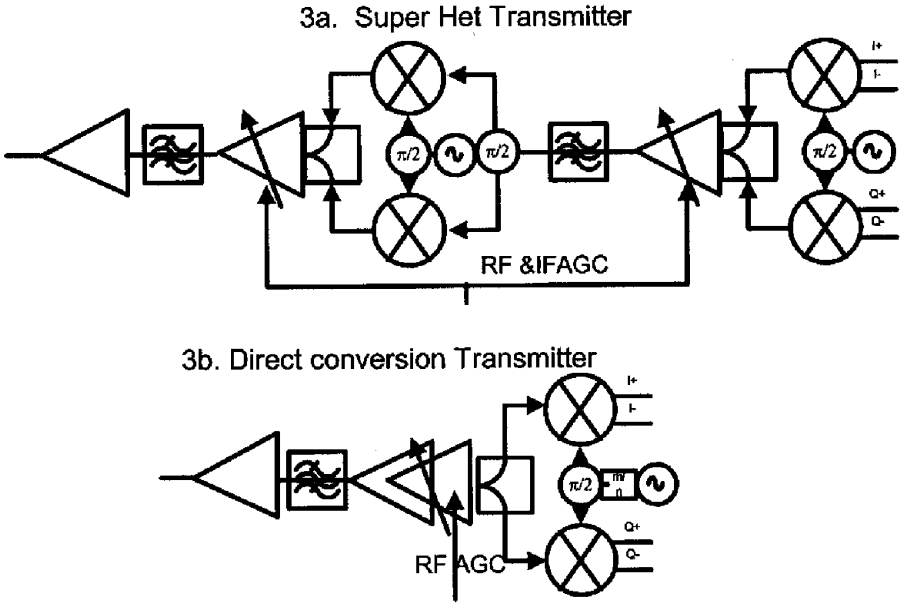

Fig. 3. (a) Super-heterodyne and (b) DCT architectures.

plans and need different IF filters consuming premium board space on small form factor phones. Direct conversion of RF signals allows channel filtering to be done at baseband where implementation of power-efficient on-chip filtering is feasible. This eliminates the need for external passive filters saving board space and cost [see Fig. 2(b)].

Since IF in a DCR is zero, there is no image frequency present, as in the case of a super heterodyne. Ideally, there is no need for an inter-stage image reject filter between the LNA and mixer in a DCR. However, RF SAW filters are still needed in full duplex CDMA and WCDMA systems where leakage of the transmitter signal in to the receiver needs to be suppressed. Since the GSM transmitter is turned off in its receiver slot, the image reject filter can be eliminated in a DCR. Channel filters in a DCR are realized at baseband frequency. Advanced filter architectures enable on-chip tuning of the filters, making it feasible to optimize RF integrated circuits (RFICs) for multistandard operation (e.g., 615 kHz for CDMA, 1.92 MHz for WCDMA, and 100 kHz for GSM).

Another inherent advantage of the DCR is that it does not need a VHF voltage-controlled oscillator (VCO) and phase-locked loop (PLL) that a conventional super heterodyne would need, saving die area and cost, as well as eliminating effects of phase noise of the VHF VCO.

The DCR has been widely implemented for GSM mobile-phone systems by several companies like Alcatel, Ericsson, Conexant, ADI, Nokia, Silicon Laboratories, Samsung, and Motorola with high levels of on-chip integration and competitive performance features. Several semiconductor companies like Infineon, Conexant, Qualcomm, ADI, Phillips, and Maxim are developing and perfecting DCR implementations for WCDMA and CDMA systems.

Some of the key implementation challenges like dc offset, second-order nonlinearity, LO leakage, gain, and phase imbalance are discussed in Section III.

B. DCT

As the name suggests, baseband IQ signals directly modulate an RF carrier at the desired transmitter frequency in a DCT. Variable RF gain stages controlled by the RF automatic gain control (AGC) signal amplify the modulated RF signal to the desired power output [see Fig. 3(b)]. RF SAW filters could be used to suppress noise floor in the receiver band before feeding the signal in to the power amplifier. This is different from the traditional dual frequency-conversion transmitter where dual LO sources are used and the required dynamic range is achieved using both the IF and RF VGAs.

Component savings in a DCT as compared to a current dual-conversion transmitter is achieved by eliminating on-chip IF VCO + PLL + tank circuit components. External LC IF filters normally used in a transmitter to reduce receive band noise can be eliminated.

Current TX architectures in CDMA handsets are based on the dual-conversion transmit chain [see Fig. 3(a)], wherein baseband IQ signals are modulated on an IF carrier followed by a VGA with >80-dB dynamic range. Amplified IF are filtered using simple *LC* tuning elements and up-converted using image-reject mixers and variable-gain driver blocks. Gain partitioning is made to achieve power control, noise floor reduction, and linearity with optimal power efficiency. RFICs with 2-3 integrated PLLs and a VHF VCO are commercially available [13]. Channel filtering and wave shaping of TX IQ signals is normally implemented in the baseband. IF filtering in a CDMA/WCDMA transmitter is only needed to suppress the receiver band noise generated in IF VGA stages. IF filters are typically simple *LC* parallel resonant tank circuits tuned at TX IF. The frequency rolloff offered by these "filters" attenuate the RX band Noise floor at TX IF + duplex spacing (e.g., $\text{Duplex spacing}_{\text{WCDMA}} = 190$ MHz; $\text{Duplex spacing}_{\text{USPCS CDMA}} = 80$ MHz) to low enough levels.

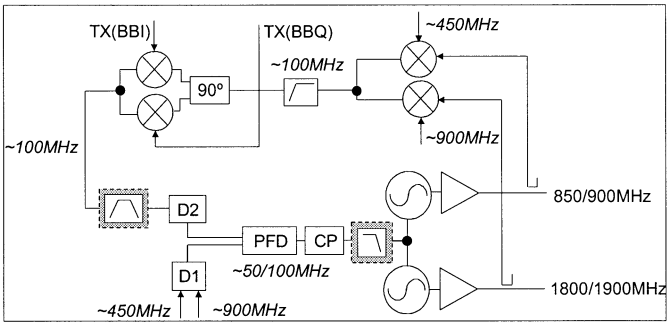

Fig. 4. Translational loop architecture for GSM transmitter.

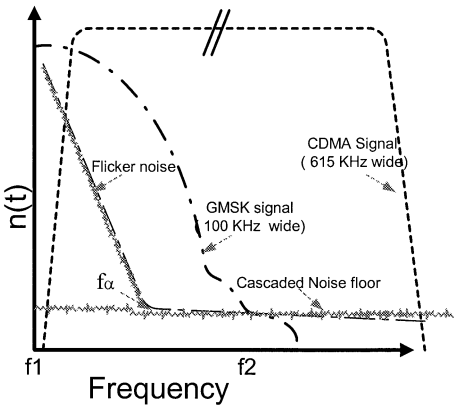

Fig. 5. Effect of flicker $(1/f)$ noise.

Transmitters in GSM handsets, wherein linearity and dynamic-range requirements are not as stringent, have successfully implemented designs based on translational loop architecture, which eliminates the need for RF SAW filter at the power amplifier's input [6]. The translational loop architecture is well suited for constant envelope modulation like Gaussian minimum shift keying (GMSK), employed in GSM systems. Operation of a translational loop is very similar to that of a standard PLL, where the VCO spectrum inside the loop bandwidth follows that of the reference oscillator. As shown in Fig. 4, quadrature transmit signals TX baseband I channel (BBI) and TX baseband Q channel (BBQ) modulate an IF, which is bandpass filtered and fed to a phase frequency detector (PFD) operating at ∼50/100 MHz. The error signal of the PFD filtered through a loop filter modulates the VCO. The loop bandwidth is kept sufficiently wide to achieve desired GMSK modulation bandwidth of 200 kHz. Sampled output of the VCO is fed back to the IQ modulator, closing the translational loop, as shown in Fig. 4. The VCO is designed to meet the out-of-band noise requirements of GSM without the need for an external RF SAW filter.

One of the key advantages of a DCT due to the absence of IF is in frequency planning of multimode systems (e.g., GSM/WCDMA) with different duplex spacing and operating frequency ranges. This task becomes more complex for a dual-conversion transmitter. On-chip tuning and programmability opens up the potential for reusability of functional blocks between different mobile-phone standards, saving die area and cost. Spurious due to m^* IF $\sim$ n^* LO are entirely eliminated as IF is zero.

Some of the key implementation challenges for the DCT are: 1) IQ phase and gain imbalance; 2) the in-band noise floor; 3) VCO pulling; 4) dynamic range; and 5) power consumption, as discussed in Section IV. The dynamic range is achieved by proper gain distribution in the baseband (analog/digital) and RF sections with associated performance tradeoffs such as variable gain in digital (requires higher DAC resolution), variable gain in analog baseband (causes increased LO leakage of mixer), and variable gain at RF (causes higher power consumption).

Several companies like ADI, Conexant, Alcatel, Nokia, Ericsson, and Silicon Laboratories have succeeded in implementing either DCT or translational loop architectures for GSM. DCT implementation for WCDMA and CDMA 2000 is actively being evaluated by industry.

III. DCR Implementation Challenges

In this section, the design issues for the DCR implementation-like effect of flicker noise, static, and dynamic dc offset, second-order nonlinearity, as well as IQ gain and phase imbalance are presented.

A. $1/f$ Noise From I/Q Mixer

Flicker noise in semiconductor devices, popularly known as $1/f$ noise, is inversely proportional to the frequency. The $1/f$ corner frequency f_α (Fig. 5) is the frequency at where flicker noise is equal to (cascaded) thermal noise floor. Flicker-noise property of a device is semiconductor processes dependant. f_α is typically in the range of 4∼8 kHz for the BiCMOS process, while it is in the vicinity of 1 MHz for MOSFET devices [1].

The noise figure of the receiver front end normally determines the ability of a receiver to demodulate the weakest of the signals. Since received signals in a DCR are directly down converted to baseband or zero IF, additional signal-to-noise degradation due to flicker noise of the down converters could be significant. At input RF signal levels close to the receiver sensitivity, the baseband IQ signal at the output of the down converter is very low. The gain provided in the LNA and the direct-conversion mixer stages, as shown in Fig. 2(a), amplifies the signal as well as noise floor at the mixer output. Effective corner frequency f_α is a frequency where flicker noise of the mixer equals the cascaded noise floor, as shown in Fig. 5.

The noise floor due to $1/f$ noise at the mixer output can be estimated as

$$n(t) = n_0 \left[(f2 - f1) + f_\alpha * Ln\left(\frac{f2}{f1}\right) \right] \qquad (1)$$

where $n(t)$ is the integrated noise for given $f\alpha$, n_0 is input referred noise floor at the down converter, and the passband of the baseband signal spectrum is $(f2 - f1)$.

For GSM signal ∼100 kHz bandwidth at baseband, the SNR degradation or effective noise figure increase in the down-converter block could be of the order of ∼1.2 dB @ $f_\alpha = 5$ kHz. Wide-band systems like WCDMA and CDMA signals have minimal energy at dc. Therefore, the relative

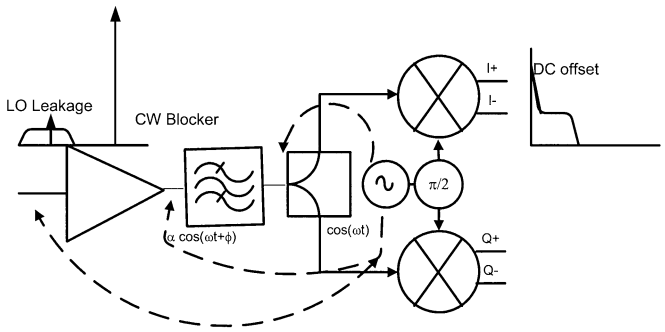

Fig. 6. Possible LO leakage paths.

degradation due to flicker noise is lower in wide-band signals. It is evident that for a given f_α, narrow-band signals (100 kHz) like GSM are more susceptible to flicker noise compared to wider band signals like CDMA 2000 (615 kHz) and WCDMA (1.92 MHz). The flicker-noise effect in GSM can be minimized by selection of right semiconductor process with low f_α and providing adequate gain in the front end to improve relative SNR at the down-converter output. The "low IF" architecture instead of the "zero IF" followed by high-pass filtering could be another technique to overcome effects of flicker noise [9].

B. DC Offset

Undesired dc offset in IQ signals shifts the origin of a baseband signal constellation, causing potential signal saturation, as well as degradation in bit error rate (BER) performance. Susceptibility of signals to dc offset depends on the type of digital modulation used. GMSK-modulated GSM signals, which have signal content near dc, are more susceptible compared to QPSK modulated spread-spectrum signals used in CDMA 2000 and WCDMA.

Static or dynamic dc offset can result due to multiple means in a DCR. The self-mixing of the LO with a phase-shifted version of itself or imbalance in signal paths due to suboptimal design are some of the known mechanisms by which static dc offsets are generated in a DCR. Sudden changes in signal level due to deep fade or LO re-radiation from a moving reflector or abrupt appearance of a blocker, etc. cause time-varying or dynamic dc offset. Essentially, dc-offset generation is a second-order phenomenon.

The nonlinearity of practical amplifiers can be depicted by

$$V_o = a_l V_i + a_2 V_i^2 + a_3 V_i^3 + \cdots \tag{2}$$

where V_i can be a combination of desired signal and multiple signals of interference.

The term $a_2 V_i^2$ represents second-order nonlinearity of the amplifier, which is one of the main causes of dc-offset generation in DCRs.

1) Static DC Offset: Offsets are typically caused due to the mixing of the LO signal with a phase-shifted replica of itself. Several coupling paths can exist on a DCR, as depicted in Fig. 6. The LO leakage amplified through the LNA and phase shifted in the RF SAW filter can mix with the LO signal at the mixer input port to generate dc, which can vary across the operating frequency band. As shown in Fig. 6, let the LO be represented by $\cos(\omega\tau)$ and the LO leakage by $\alpha\cos(\omega\tau + \phi)$, where α is the relative gain in the leakage path and ϕ is the relative phase shift of the coupled LO.

The self-mixing of the LO signal can then be represented by

$$\cos(\omega\tau) * \alpha\cos(\omega\tau + \phi) \Rightarrow \cdots + \frac{\alpha}{2} * \cos(\phi) + \cdots \text{ in I channel} \tag{3}$$

$$\mathrm{Sin}(\omega\tau) * \alpha\cos(\omega\tau + \phi) \Rightarrow \cdots + \frac{\alpha}{2} * \mathrm{Sin}(\phi) + \cdots \text{ in Q channel.} \tag{4}$$

As seen from the above equations, the desired signal levels are much lower compared to the LO level in a receiver, making it more challenging to contain dc offsets within acceptable limits. Circuit imbalance in IQ paths that result due to practical limitations of semiconductor process and or layout constraints of the IC can also cause dc offsets.

2) Dynamic DC Offset: Varying channel conditions resulting from multipath fading, mobility of handset, and abrupt channel degradation due to sudden shading of the direct signal path can cause time-varying or dynamic dc offset. The AGC loop of the receiver tends to rapidly adjust receiver gain to maintain signal levels constant in such conditions. DC offsets generated by such gain changes can cause burst errors in the receiver before being calibrated out by an offset correction loop in system. DC offset is further amplified by a high-gain baseband IQ signal path.

Current DCR architectures employ several methods to contain and calibrate signal impairment due to dc offset. Wide-band signals as defined in CDMA or WCDMA standards have almost no signal energy near dc. Capacitive coupling of the IQ baseband signals can remove dc offset without causing signal-to-noise degradation. Narrow-band GSM signals have energy at dc, hence, capacitive coupling may not be an option. Typically, dc offsets measured in an idle mode can be subtracted from the actual RX slot in TDMA systems. However, "wandering dc offset" caused by intermittent blockers can be a concern. Dynamic calibration of dc offset and digital signal processing (DSP) techniques to calibrate dc are some other popular techniques employed to minimize signal degradation.

Preventing dc offset by providing adequate linearity can, of course, alleviate most of the problems. Innovative circuit designs with accurate matching and semiconductor process technologies with deep trench isolation can minimize on-chip coupling of the LO. Package isolation and careful board layout are also important in designing a DCR with minimal LO leakage.

Fig. 7 indicates some of the techniques like sub- or superharmonic down-conversion schemes that are employed to prevent leakage of the LO signal with in-signal bandwidth at receiver input. The LO is at either harmonically ($n^* f_{LO}$) or subharmonically ($1/m^* f_{LO}$) related to the desired RF. Adequate on-chip isolation from down converter to receive path minimizes leakage of the LO at the same frequency. Other schemes employ a variable ratio ($m/n^* f_{LO}$) division to ensure offset of the VCO frequency from the desired signal [2], [4].

DC-offset calibration techniques presented in several papers [1], [2] include compensation schemes using digital sample and

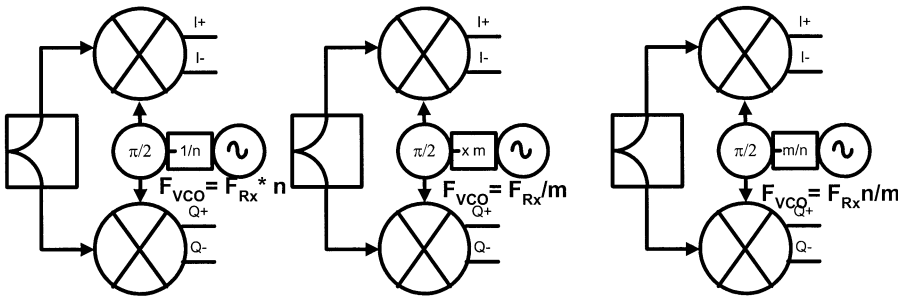

Fig. 7. Various LO schemes to prevent leakage at RX frequency.

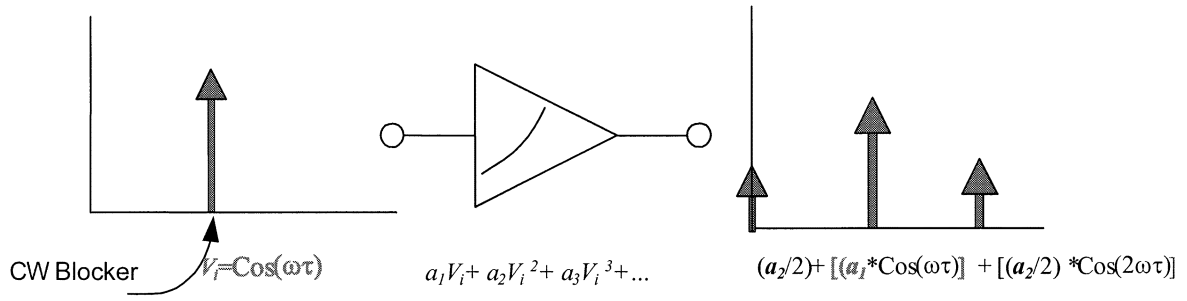

Fig. 8. DC offset due to a CW blocker.

hold feedback, offset estimation in the baseband with a correction signal fed back to the receiver, dc-offset estimation on a burst-to-burst basis in a GSM system, etc. Servo loops can be employed to minimize offsets in the DCRs for wide-band signals [3] where cancellation of signal energy within the loop bandwidth does not cause significant signal degradation.

The "sequential dc-offset calibration scheme" wherein dc offsets are estimated and calibrated independently in multiple gain blocks, has been reported [5]. Less than 6 mV of corrected offset was achieved employing this technique.

C. IIP2 Requirement

IIP2 is a useful metric to quantify second-order distortion products of a receiver. It is a virtual power in dBm at which the fundamental $P\text{in}$ versus $P\text{out}$ slope intersects that of IM2 or second-order intermodulation products. IIP2 is of particular significance in a DCR as second-order nonlinearity effects can down convert continuous wave (CW) as well as AM modulated blockers to dc or near dc, causing SNR degradation. Fig. 8 depicts how a CW blocker generates dc in an amplifier with poor second-order nonlinearity (IIP2).

The second-order term of (2) can be expanded to illustrate generation of dc due to a CW blocker. Let $V_i = \cos(\omega\tau)$ be the input CW blocker. Then

$$a_2 V_i^2 \Rightarrow a_2\left[\cos(\omega\tau)\right]^2 \Rightarrow \left(\frac{a_2}{2}\right) + \left[\left(\frac{a_2}{2}\right) * \cos(2\omega\tau)\right]. \tag{5}$$

Similarly, it can be shown that multiple CW jammer signals can generate interference within the desired channel bandwidth. For example, in the CDMA channels sharing the same cellular 800-MHz frequency band as AMPS (Analog Systems), the presence of multiple narrow-band AMPS channels @ $\omega 1$ and $\omega 2$ where $(\omega 1 - \omega 2)$ is $<$ CDMA signal BW, can result in interference. The IIP2 requirement of the down converter needs to meet such operating conditions in the field even though the minimum performance requirement of the CDMA system does not stipulate such a test.

The AM suppression requirement in the GSM also mandates the handset receiver to tolerate an AM blocker @-31 dBm without significantly degrading the receiver. The GSM receiver, for example, needs to tolerate the CW blocker @-31 dBm with signal level $= -99$ dBm as follows:

$$\text{IIP2} = 2 * P\text{in} - (\text{IM2} + 3\,\text{dB}). \tag{6}$$

Since the minimum SNR for 0.001 BER is 9 dB for the GSM, the tolerable $\text{IM2} = (-99 - 9)$ dBm $= -108$ dBm. Therefore, the IIP2 required is

$$2 * (-31) + 108 - 3 = 43\ \text{dBm}.$$

In wide-band systems like CDMA and WCDMA, where ac coupling is possible to overcome dc offsets, IIP2 is still critical in view of the fact that the modulated blocker or TX leakage can also down convert to the baseband (Fig. 9). The modulated blockers in the downlink consist of several channels with composite signal crest factors of $\sim$12 dB in WCDMA. In addition, the leakage of the uplink transmitter through the duplexer at the LNA presents undesirable interference with large envelope variation. The second-order nonlinearity of the receiver generates interference at the baseband. Maintaining high IIP2 is a common requirement for GSM and CDMA, as well as WCDMA DCRs.

Similarly, it can be shown that a modulated blocker can also produce noise at dc or the baseband. Let $(1 + m * (H_t))\cos(\omega t)$

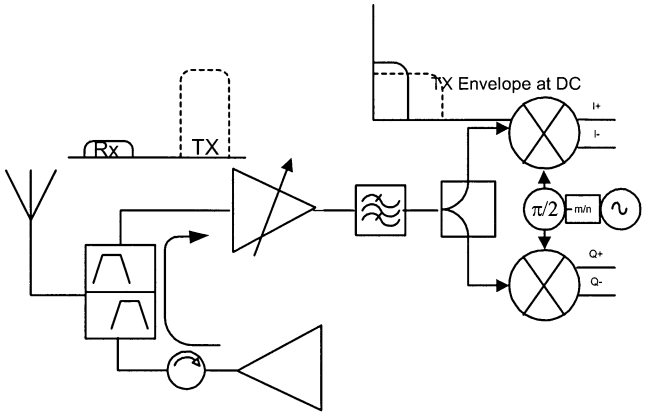

Fig. 9. Second-order nonlinearity of receiver down converts TX leakage to dc.

be a modulated blocker with an equivalent AM modulation index "m" and complex envelope $H(t)$. Then

$$a_2\Big[\big(1+m*(H_t)\big)\cos(\omega t)^2\Big] \Rightarrow a_2\left[\ldots+\frac{1}{2}m*H(t)+\frac{m^2}{2}*(H_t)^2\cdot\big(1+\cos(2\omega t)\big)+\cdots\right]. \quad (7)$$

Power in the demodulated envelope of the interference $= a_2^2[1/2 + m*H(t) + m^2/2*(H_t)^2]^2$ is at dc causing SNR degradation.

In general, the second-order nonlinearity of a receiver (IIP2) can be calculated to be

$$\text{IIP2} = 2*\text{Tone} - \text{IMOD} - 10*\log\left(\frac{m^2}{2}\right) - 3 \quad (8)$$

where "Tone" indicates power in the jammer tone, "m" is the equivalent AM depth, and "IMOD" is the maximum tolerable interference energy to achieve desired BER in the receiver. Three decibels is subtracted from the IIP2 equation since half the power falls out as the baseband spectrum occupies twice the signal BW.

IIP2 in a DCR can be improved by designing circuits with high common-mode rejection, near perfect balance between differential arms of IQ signal paths, as well circuit topologies to improve phase quadrature between the I and Q signals. Also, the even harmonic mixer architecture, wherein generation of even-order products is minimized, has been published with significant improvement in effective IIP2 [4].

Novel calibration techniques [5], [6] have also been used to enhance IIP2 performance significantly Fig. 10 shows measured data, demonstrating signal quality improvement due to enhanced IIP2 [6]. The desired signal at -99 dBm is combined with a CW interference and is applied to a GSM receiver (CX 74017). Power of the CW interference is swept from -30 to -24 dBm (Trace 3 in Fig. 10). Trace 1 is the demodulated signal impaired by dc offset due to the CW interference before calibration. Trace 2 is the demodulated signal after IIP2 calibration to improve signal quality in the presence of a strong jammer signal.

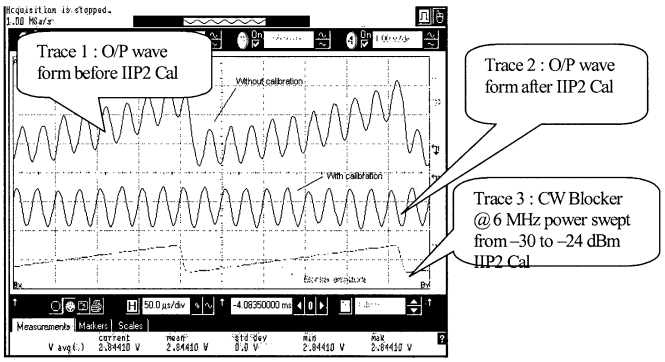

Fig. 10. Measured data on improvement of IIP2 due to calibration on a DCR [6].

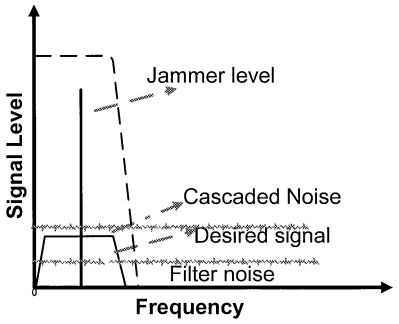

Fig. 11. Dynamic range of baseband filters.

D. Noise Floor of the Baseband Channel Filters

The baseband channel filter needs to handle large jammer tone (J), while preserving the SNR of the desired signal. Fig. 11 gives a pictorial representation of signal, jammer, and noise levels referred to the input of the filter. Dynamic range of the baseband filter depends on the peak level of the jammer tone and input referred noise floor of the baseband filters. The filter noise floor needs to be much lower than the cascaded noise floor of the receiver front end such that the cascaded noise figure of the receive path is not degraded due to the filter.

Several channel filter architectures are implemented using g_mC, active *RC*, and switch cap architectures. The tradeoff between different options include dynamic range, input referred noise floor, and tuning requirements. The "g_mC" filters are known to have low noise floor ($2 \sim 4n$ V/$\sqrt{}$ Hz) and relatively simple tuning, but poor capability to handle large signals. The switched cap filters have good linearity and accurate channel selectivity, but noise floor is typically close to 20 n V/$\sqrt{}$ Hz and could be a concern. An active *RC* architecture offers an optimal dynamic range performance for CDMA and WCDMA systems where the jammer level could be $>$ 71 dB above the desired signal. Decent input referred noise floor close to 6 n V/$\sqrt{}$ Hz could be achieved for reasonable resistor values [2], while filter tuning poses moderate implementation challenge.

Idle slots can be used for filter tuning and calibration in TDMA systems like GSM. Full duplex systems like CDMA/WCDMA need to receive signals continuously, hence, calibration could be done when the device is powered on to achieve an acceptable channel filter profile. On-chip calibration of a bi-quad WCDMA channel filter achieving a tuning range of $\sim +/-20\%$ has been presented. [9]

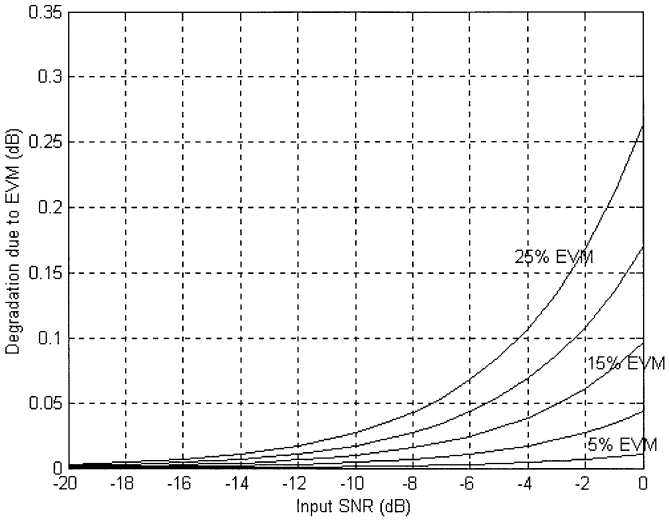

Fig. 12. Effect of EVM on SNR.

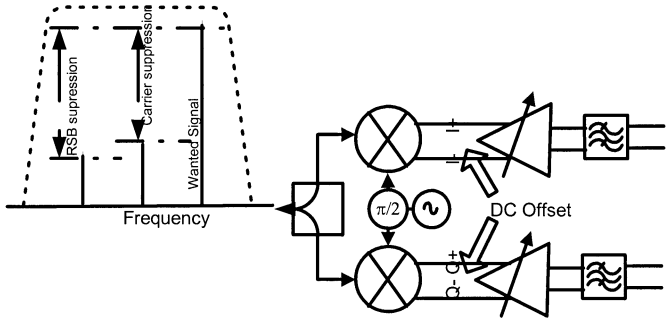

Fig. 13. Gain control in baseband could cause poor carrier suppression.

It is evident from Fig. 13 that a higher front gain prior to the filters would increase the cascade noise floor and reduce the effect of the filter noise floor, but the jammer level at the input of filters would increase correspondingly. The tradeoff between achievable dynamic range and acceptable cascaded noise-figure degradation due to filter noise floor of the receive chain needs to be made to arrive at an optimal receiver architecture.

E. Phase and Gain Mismatch of IQ Paths

Gain and phase mismatch between the I and Q channel filters and amplifiers with large cascaded gain can cause asymmetry and rotation in the signal constellation resulting in error vector magnitude (EVM) degradation. Tolerable gain and phase imbalance depends on modulations techniques employed in a system.

Inherent processing gain offered in spread-spectrum systems reduce susceptibility to a certain level on de-spread symbols. Degradation of modulation accuracy or EVM of receive signals can be modeled as a ratio of powers of the error and reference vectors.

$$\text{EVM} = \sqrt{\left(\frac{P_e}{P_r}\right)} \tag{9}$$

where P_r is the ideal reference vector P_e is the error vector resulting due to a combination of residual sideband (RSB) and carrier feed through due to impairments like gain and phase mismatch.

Fig. 12 depicts degradation in the SNR due to EVM resulting from gain and phase imbalance at different tolerable input

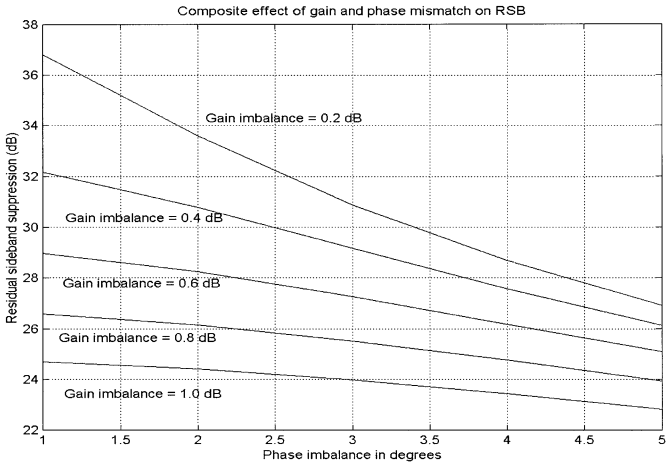

Fig. 14. RSB suppression versus gain and phase imbalance.

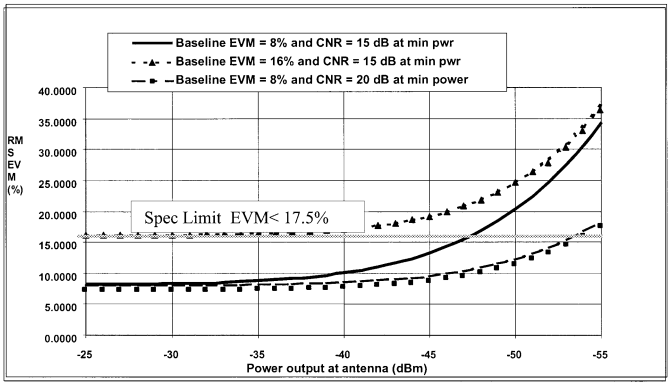

Fig. 15. EVM as a function of output power for a WCDMA system.

SNRs, which again is dependent on demodulation schemes and receiver processing gain.

For example, minimum-input SNR for WCDMA at sensitivity is ~ -7 dB, while CDMA SNR is ~ -1 dB @ sensitivity. Degradation due to 15% EVM is $\sim <$ 0.05 and .075 dB, respectively. Accurate gain tracking is achieved by symmetrical layout and identical circuit topologies with minimal relative process variation in I/Q paths.

Methods to address phase imbalance like differential poly phase splitters and quadrature VCOs have been discussed in detail in several papers, including [7]–[10]. Feasibility of on-chip VCOs at double or quadruple of receive frequencies makes it possible to use digital dividers to generate accurate phase quadrature at RF [8].

IV. DCT Challenges

Common architectures for mobile phones transmitter implementation include: 1) double conversion from baseband to IF and IF to the final RF frequency; 2) direct up conversion from baseband to RF in one step; and 3) offset PLL or translational-loop-based architectures used for constant envelope transmitter modulation.

Double-conversion architecture requires an IF VCO and PLL, and multimode multiband systems make this more challenging

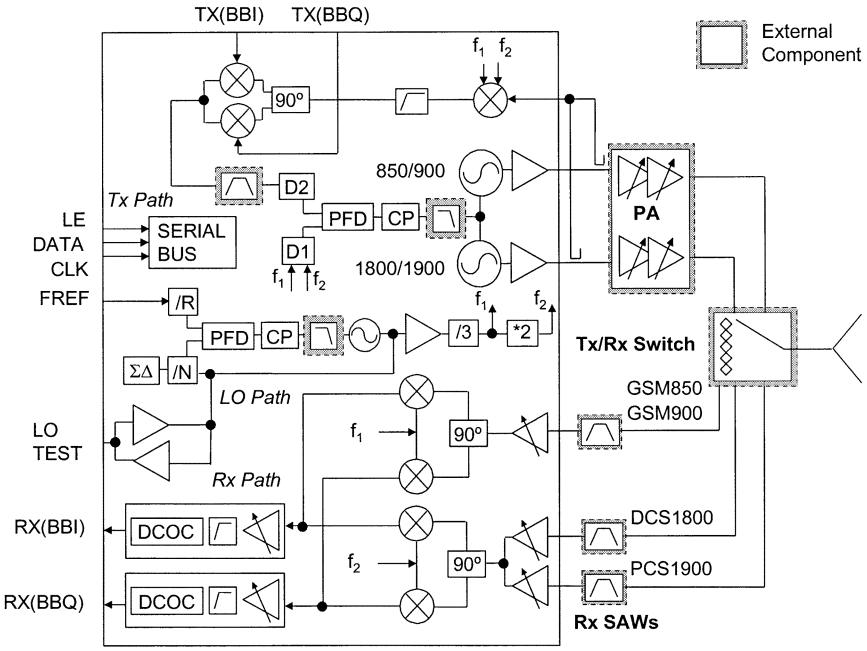

Fig. 16. Block diagram of a quad-band GSM transceiver (CX 74017).

in terms of spurious generation and frequency planning. Translational loop architecture is mostly suitable only for constant envelope modulation schemes like GMSK used in GSM mobile phones. However, it is challenging to implement this architecture with enhanced data rate through GSM evolution (EDGE) and CDMA (8PSK and QPSK) like modulation schemes. Direct modulation offers the benefit that it can be used in combined multimode systems and avoids the need for the IF VCO and PLL. However, the DCT has unique implementation challenges, as outlined below.

A. IQ Phase and Gain Imbalance

EVM of an IQ modulator is an important metric that determines the transmit signal integrity. RSB and inadequate carrier suppression in IQ modulators are the main impairments that increase energy in the error vector.

Phase and gain imbalance in the in-phase and quadrature-phase arms of the modulator produce unwanted RSB. It is expressed as follows:

$$\mathrm{RSB(dB)} = 20 * \log_{10} \sqrt{\left[\frac{\left(K^2 - 2K\cos\Phi + 1\right)}{\left(K^2 + 2K\cos\Phi + 1\right)}\right]} \qquad (10)$$

where K is the linear amplitude imbalance between the I and Q channels and Φ is the phase imbalance in degrees or deviation from perfect phase quadrature.

The dc offset between $I+$ and $I-$ or $Q+$ and $Q-$ can result in undesired carrier component in the spectrum. For an rms signal "S" and dc offset of "v," the carrier suppression is expressed as

$$\text{Carrier suppression (dBc)} = 20 * \log_{10}\left(\frac{v}{S}\right). \qquad (11)$$

It is also feasible to realize part of the linear power control dynamic range needed for WCDMA, and CDMA DCTs in the baseband amplifier and filter blocks, as shown in Fig. 13. While it simplifies the dynamic range requirement of RF stages, additional dc offsets generated in the variable gain baseband stages need to be compensated or calibrated. The relative residual dc offset at the input of the direct modulator can lead to lower carrier suppression.

Fig. 14 below indicates the RSB suppression as a function of gain and phase imbalance in a DCT. For $\Phi = 2^\circ$ and $K = 0.2$ dB, the RSB is $\sim$33.5 dB

For implementation shown in Fig. 13, baseband signal IQ swing needs to be kept as large as possible to maximize carrier suppression. For a given dc-offset, energy in RSB, as well as carrier add to the error vector degrading EVM. In CDMA systems, the "ρ factor" is used as a metric to define waveform quality, while EVM is used to define quality of a WCDMA waveform. ρ and EVM are related by

$$\rho = \frac{1}{\left(1 + \mathrm{EVM}^2\right).} \qquad (12)$$

The modulator is at RF frequency in the DCT. Maintaining signal quadrature over a wide frequency range, especially for multisystem architectures, is a challenge that needs careful layout, circuit balance, and calibration techniques.

B. VCO Pulling and Remodulation

A strong modulated signal at the same frequency as the LO can cause pulling of the VCO, introducing increase in phase noise, and leading to poor waveform quality. Shielding and isolation can alleviate this problem to some extent. Proximity of high-power stages in a practical handset makes it challenging to

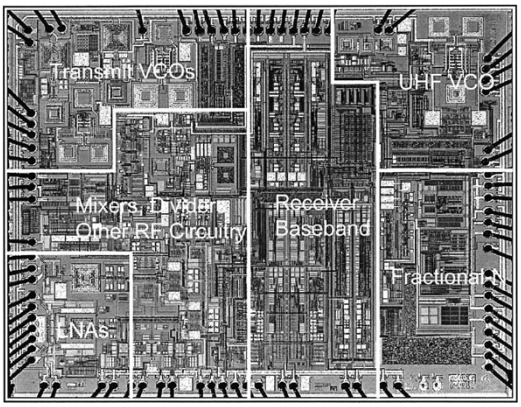

Fig. 17. Microphotograph of the quad-band GSM radio.

achieve desired isolation by mechanical shielding. An on-chip VCO operating at double or even quadruple of the desired transmitter frequency followed by digital dividers can eliminate VCO pulling and achieve acceptable phase quadrature required for the IQ modulators. Improved on-chip isolation by using deep trenches on the silicon substrate and offset VCO schemes are also popular in eliminating pulling or remodulation of the VCO [9]. A CMOS implementation of WCDMA direct modulation using a VCO at double the desired frequency has been reported [8].

C. Dynamic Range and Power Consumption

A transmit power control range of GSM handsets is required to be of the order of 30 dB, while CDMA/WCDMA systems mandate a 90-dB accounting margin for the temperature and process variations of functional blocks. In most of the popular GSM transmitter architectures employing an offset VCO or translational loop [2], [6], which provide fixed output from the VCO, power control is achieved by controlling RF gain of the nonlinear power-amplifier stage. However, future systems based on enhanced data rates for GSM evolution (EDGE) need a linear power amplifier, enabling the need for controlling the DCT output to achieve required transmit dynamic range.

System design requirements for WCDMA and CDMA standards mandate accurate power control of mobile handsets so as to ensure that the signal received from all mobile handsets in the cell is equal. The base-station sends a periodic power control bit to increase or decrease its power such that the SNR is just enough for demodulation. As compared to a conventional dual-conversion transmitter where the dynamic range is split between IF and RF stages, the DCT needs to achieve most of the dynamic range at RF. This is likely to result in extra power in RF blocks, which may be somewhat offset by the fact that IF amplifiers and filters are totally eliminated in the DCT. One way to realize the power control range is to split the gain control between RF and baseband stages [8]. While this architecture is similar in concept used in dual-conversion transmitters [13] and more power efficient, as well as easier to implement, it may need careful design and dc-offset control and calibration to achieve acceptable carrier leakage issue.

Statistical studies conducted by the CDMA development group (CDG) for various field conditions indicate that distribution of average power transmitted by CDMA handsets is far lower than its maximum power output. Improving the efficiency of the transmit chain is, therefore, important in extending talk time of the handsets. Power consumption of the transmitter can be gracefully reduced as a function of power level by using class-AB amplifier stages in combination with current steering techniques [9], [13].

TABLE II
KEY PERFORMANCE SUMMARY

Receiver	850/900MHz	1800MHz	1900MHz
NF	3.1dB	3.6dB	4.1dB
LO re-radiation	-110dBm	-105dBm	-103dBm
IQ phase match	1°	1°	1°
IQ amplitude match	0.5dB	0.5dB	0.5dB
Typical sensitivity	-109dBm	-107dBm	-107dBm
Sensitivity with blocker	-105.5dBm	-104dBm	-104dBm
IIP2 over channels (cal.)	> 50dBm	> 50dBm	> 50dBm
3dB baseband BW	98kHz	98kHz	98kHz
Group delay to 100kHz	< 0.3μs	< 0.3μs	< 0.3μs
Rejection at 3MHz	> 120dB	> 120dB	> 120dB
Power (incl. Synth.)	75mA	80mA	80mA

Transmitter	850/900MHz	1800/1900MHz
Phase error	1.5°	1.6°
400kHz noise	-64dBc/30kHz	-65dBc/30kHz
20MHz noise	-164dBc/Hz	-158dBc/Hz
Power (incl. Synth.)	130mA	120mA

Synthesizer	1200-1700MHz
Phase noise @ 400kHz	-124dBc/Hz
Phase noise @ 3MHz	-141dBc/Hz
Lock time	< 175μs
Power	35mA

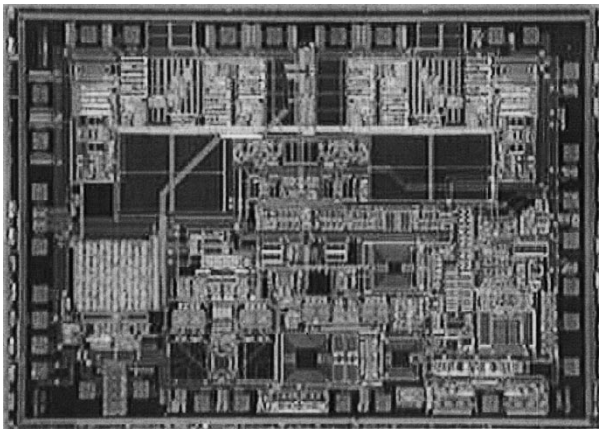

Fig. 18. Microphotograph of Analog Device's Othello IC.

D. In-Band Noise Floor at Low RF Power

Signal quality as defined by the "ρ factor" or EVM is set by the carrier-to-noise ratio (CNR) at minimum controlled output power. Fig. 15 indicates degradation in the EVM versus SNR @ minimum controlled power for a WCDMA transmitter [14]. The EVM in a transmitter chain is typically due to cascaded impairments in several blocks including the baseband, IQ modulators, LO, and power amplifier. WCDMA performance specification mandates EVM of the entire TX chain to be $<$17.5%. The baseline EVM indicates typical EVM of the TX chain at

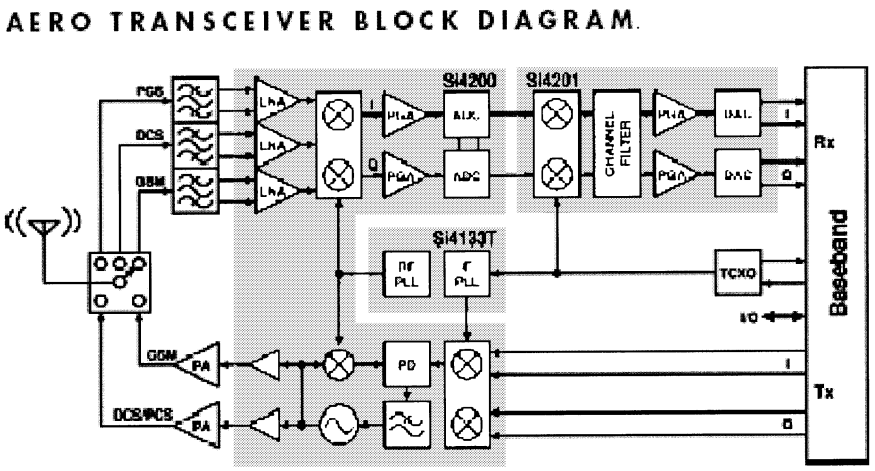

Fig. 19. Block diagram of Silicon Laboratories low IF receiver for GSM/DCS and PCS.

higher power. The effect of EVM degradation for different CNR is indicated by different traces in Fig. 15. For example, if a transmitter chain with a baseline EVM of 8% (spec. margin of 9.5%) achieves a CNR of 20 dB at minimum TX power, the EVM is within the spec limit for any $P\text{out} > -60$ dBm. However, for the same transmitter, if the in-band noise is higher or the CNR is 15-dB, the EVM spec compliance is ensured only for $P\text{out} > -47.5$ dBm.

In CDMA, WCDMA systems power control range varies from maximum power at a limiting cell range to minimum power (-50 dBm) for mobile handsets at close proximity to the base station. Entire dynamic range (>90 dB) may be achieved in the direct conversion mixer and driver stages. As the power of the DCT is reduced through close loop control, RF blocks act more like an attenuator, thereby reducing in-band noise floor. The CNR of >20 dB is achievable by optimal design of IQ modulators and driver amplifiers.

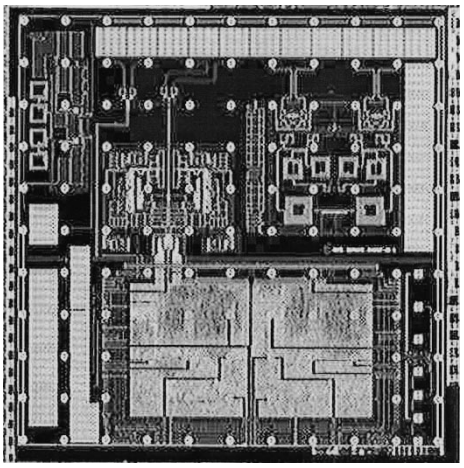

Fig. 20. Microphotograph of DiTran's CDMA DCR using RF CMOS process.

V. DCR/DCT Examples and Measured Performance

DCRs and transmitters have been in commercial use for GSM mobile phone systems. Several companies including Qualcomm, Infineon, Skyworks Solutions Inc., Conexant, DiTran, Phillips, Maxim, ADI, and others are actively pursuing DCR and DCT implementations for WCDMA and CDMA 2000 systems. At the time of publication of this paper, there are very few commercially available chipsets. Some of the popular RFIC implementations are presented below with a brief list feature set as have been publicly made available by their respective companies.

A. Example 1: Tri-Band Direct Conversion BiCMOS Transceiver (Skyworks Solutions Inc.) [6]

Skyworks Solutions Inc. (formerly Conexant Systems) has developed a single-chip GSM direct conversion transceiver ASIC, which includes a receiver, fractional N synthesizers, on-chip VCOs, and transmitter chain. This device is designed in a BiCMOS process for triband GSM/GPRS applications. The receiver is based on zero IF architecture with on-chip IQ filtering and programmable gain amplifiers. Proprietary design and calibration techniques achieve high IIP2 and low dc offsets. The transmitter is based on an offset PLL or translational loop, eliminating the need for RF SAW filters before the power amplifier. Fractional N frequency synthesizer and on-chip VCOs are designed to provide spectral purity and frequency agility needed to meet GSM system requirements. A block diagram of the device and microchip photograph are shown in Figs. 16 and 17, respectively. Key performance summary of the receiver, transmitter, and synthesizer blocks are tabulated in Table II [6].

B. Example 2: Othello IC (Analog Devices) [16]

Othello is an integrated transceiver with a super homodyne (direct conversion) receiver and Virtual IF or translational loop transmitter. The RFIC is implemented in a 0.6-μm BiCMOS process designed to target GSM radio requirements for 900-, 1800-, and 1900-MHz applications. A microphotograph and block diagram of the device is shown in Fig. 18.

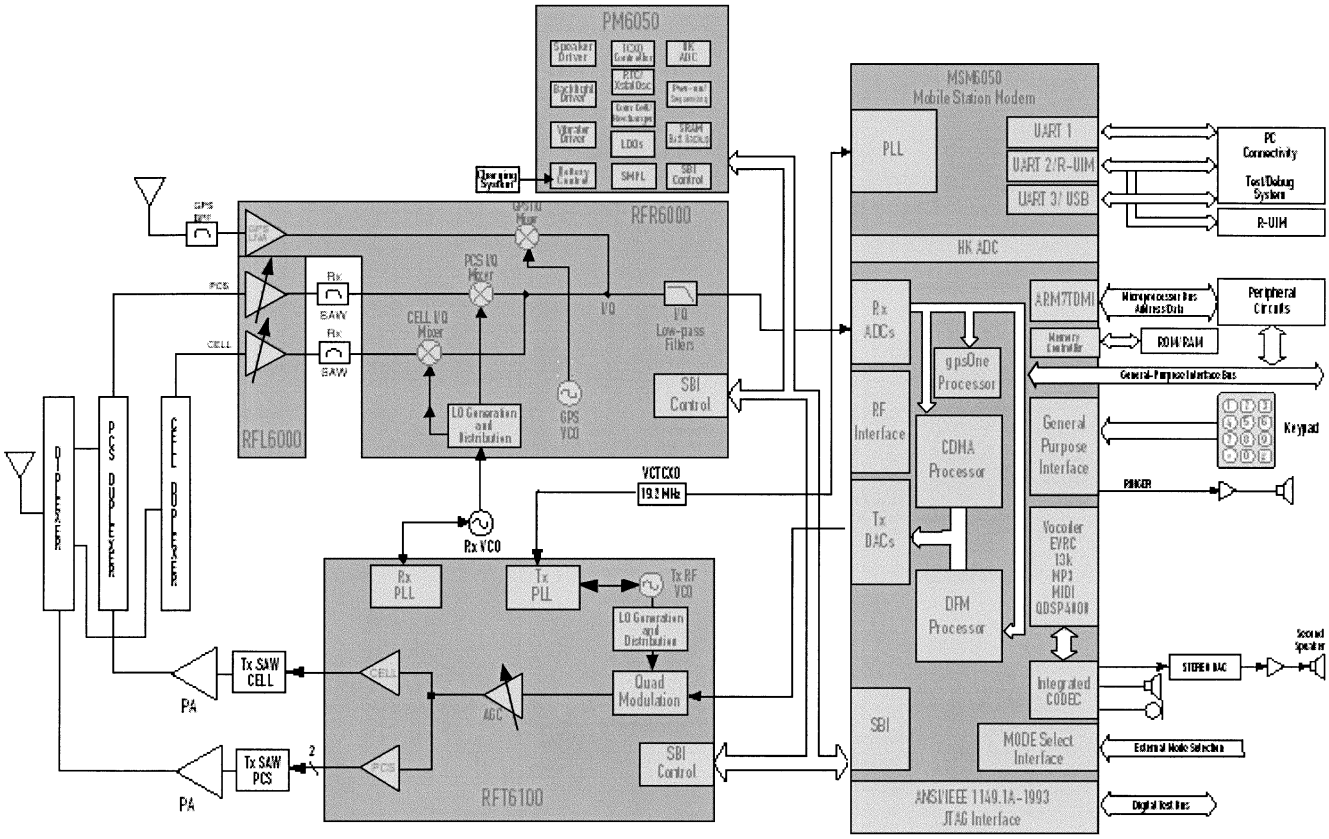

Fig. 21. Qualcomm's direct conversion CDMA/AMPS/GPS radio for trimode quad-band applications.[2]

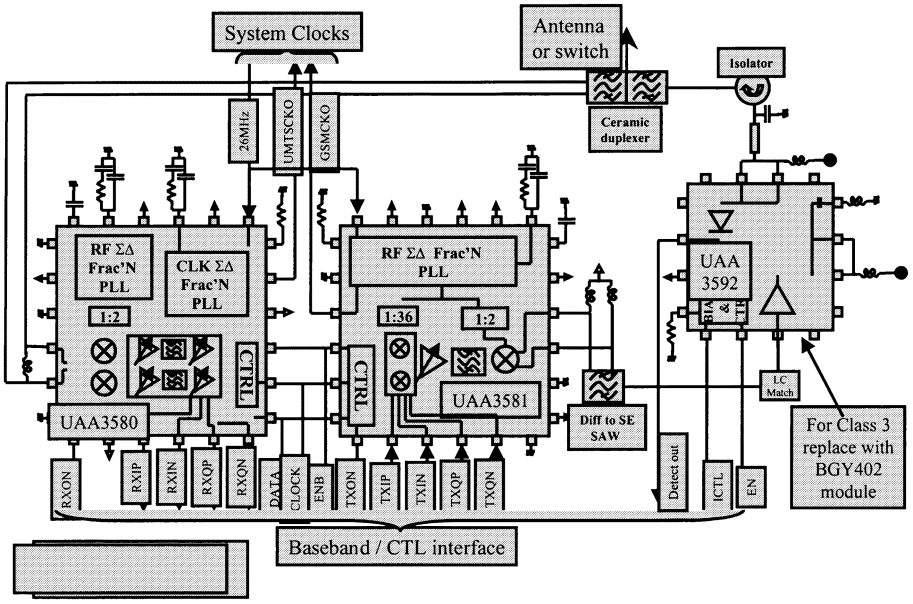

Fig. 22. Block diagram of Bi CMOS WCDMA radio [16].

C. Example 3: CMOS Low IF Transceiver for Triband GSM (Silicon Laboratories)[1]

Direct conversion transceiver designs in the CMOS process could be more cost effective as compared to similar architecture implemented on SiGe or BiCMOS. Known challenges like $1/f$ noise due to a higher f_α corner compared to bipolar or SiGe devices need to be addressed. Down conversion to low IF instead of zero IF can circumvent degradation due to $1/f$ noise, dc offsets, and IIP2 requirements. Silicon Laboratories implemented

[1][Online]. Available: http://www.silabs.com/pdfs/FinalAeroPB.pdf

[2][Online] Available: http://www.cdmatech.com/solutions/pdf/msm6050_chipset.pdf

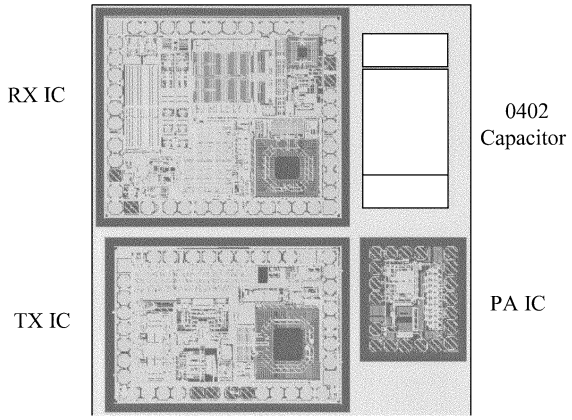

Fig. 23. Microphotograph of BICMOS radio chipset [16].

a highly integrated transceiver using a low IF receiver and offset PLL transmitter (Fig. 19).

D. Example 4: CDMA DCR "Jazz" (DiTrans Corporation) [15]

The "Jazz" receiver (Fig. 20) is essentially a digital direct conversion RF CMOS IC designed by the DiTrans Corporation for cellular CDMA and personal communication system (PCS) CDMA, as well as AMPS application. The device includes fully integrated LNA, VCO, A/D, and baseband filters. The device is advertised to achieve -109-dBm sensitivity in cellular and PCS CDMA modes and -120-dBm sensitivity in AMPS mode.

E. Example 5: CDMA DCT and DCR Chipset (Qualcomm)

Qualcomm announced development of a family of DCR and transmitter chipsets for different applications catering to CDMA, WCDMA, and GSM cellular standards. One of the chipset block diagram, shown in Fig. 21, is designed to cater to triband quad-mode (cell CDMA, cell AMPS, PCS CDMA, and GPS) applications. The receiver ASIC RFR 6000 series device is a DCR for cellular and PCS CDMA and cellular FM applications. GPS VCOs, LO generation blocks, as well as direct-conversion mixers are integrated in the device. The receiver needs external RF SAW filters for cellular and PCS bands and only one external VCO for cellular and PCS CDMA/AMPS modes. LNAs are included in the separate package RFL 6000. The transmitter device RFT 6100 is announced to include a DCT chain form IQ input to driver output covering cellular CDMA and PCS CDMA requirements. The device also integrates two synthesizers for RX and TX, on-chip TX VCOs, and direct up-converter blocks. A block diagram of the DCR and transmitter is shown in Fig. 21.

F. Example 6: Bi CMOS Implementation of WCDMA Radio Chipset. (Phillips Semiconductors) [16]

Phillips Semiconductors has announced development of wide-band CDMA radio consisting of a DCR, transmitter ASIC, and power amplifier. All the parts are designed using a "QUBIC4" Bi CMOS process featuring deep-trench isolation, 40-GHz Ft, and high-density ($5\ \mathrm{fF}/\mu\mathrm{m}^2$) metal–insulator–metal (MIM) capacitors. Published DCR performance data claims a 2.7-dB noise figure, IIP2 of 48 dBm, and IIP3 of -8 dBm. A receiver integrates most of the functional blocks like LNAs, down converters, filters, and I–Q AGC amplifier chains. A transmitter ASIC employs classic offset PLL architecture to avoid LO pulling/remodulation. The transmitter device claims to meet linearity requirements of 3rd Generation Partnership Project (3 GPP) at 5.5 dBm consuming ~ 124 mA at maximum output power.

A power amplifier IC has been published to achieve 24.5-dBm output with an adjacent channel leakage ratio of 35 dBc and power-added efficiency (PAE) of 35%. A block diagram of the radio subsystem and die pictures are shown in Figs. 22 and 23.

VI. Conclusion

Key receiver implementation challenges like dc offset, $1/f$ noise, I–Q phase, and gain imbalance have been explained. Important DCT challenges like EVM, power control, and noise requirements have been discussed. A detailed discussion on challenges and some of the techniques employed to overcome these impairments have been presented. Examples of some of the leading commercially available DCR and DCT chipsets for mobile-phone applications are presented.

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Mr. Loke was the recipient of the 1997 Rockwell Semiconductors Engineer of the Year Award.

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